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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,200	03/08/2001	Kenji Shimazaki	61282-011	4112

7590 01/04/2007

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/801,200	SHIMAZAKI ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-34 and 36 are pending. Claims 35 and 37 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 5 October 2006 have been fully considered but they are not persuasive.

i. The Examiner notes that information disclosure statement filed 10/10/2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. This was addressed in the Office Action dated 5 July 2006.

ii. In the 35 U.S.C. 112 rejections made in Office Action dated 5 July 2006, the Examiner stated (emphasis added), "The following is a non-exhaustive list of the 35 U.S.C. 112 second paragraph violations in the claims." The Examiner thanks the Applicant for amending the claims and providing supporting arguments, and notes that selective portions of the 112 rejections have been withdrawn. However, the Examiner respectfully asserts that the amended claims are not sufficient to overcome all rejections made. In the 112 rejections below, the Examiner has addressed the outstanding and additional violations.

iii. The Applicant submits with regard to the first limitation of claim 1, "...the Office Action has merely concluded that the claimed invention would have been obvious based on the Examiner's own ***opinion.***" **The Examiner maintains that it would have been obvious to a skilled artisan to perform the FFT by allocating a discrete analysis frequency in**

each range. The Applicant appears to be claiming the fundamental rules of performing FFTs, as it is well known in the art that prior to performing a FFT, it is necessary to divide the signal into adequately defined bins, each with a clear frequency range. See for example, **Diethorn (US Patent No. 6,035,048) column 5 line 66 – column 6 line 6,** which states:

> The N-vector of windowed data is then subjected to N-point FFT 150. As noted,, this transform is effectuated, in our current implementation, using the DFT algorithm. Each frequency bin output from the DFT represents one new complex time-series sample for the sub-band frequency range corresponding to that bin. The bandwidth of each bin, or sub-band time series, is given by the ratio of sampling frequency to transform length.

The Examiner notes that it is known that a DFT produces the same result as an FFT but eliminates redundant calculations. Diethorn discloses performing FFTs using the DFT algorithm (i.e. a standard algorithm that is well-known in the art), which involves multiple frequency bins, each with a unique frequency range. See also **"Engineer to Engineer Note" section 3 'Points in FFT'** which states:

> An FFT output can be thought of as a series of bins at specific frequencies evenly spread over the range 0 to f/2 (f is the sampling frequency) with the space of f/N.

iv. Applicant submits, "Claim 20 recited 'calculating a correction coefficient; and ...correcting, by using the correction coefficient.' Claim 26 similarly recited 'calculating a correction coefficient.' Applicants respectfully point out that the Office Action does not address these limitations". The Examiner notes that in the previous Office Action, both these claims were rejected under 35 U.S.C. 112 for failing to define the phrase 'calculating the correction coefficient by performing processing according to a mathematical expression prepared in advance.' Based on the Applicant's supporting

arguments, the Examiner withdraws the 112 rejections and interprets a correction coefficient to incorporate the resistance, capacitance, and power of the circuit.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 13-19 are rejected under 35 U.S.C. 112, first paragraph, for undue breadth. The claim contains a single means. See MPEP 2164.08(a):**

A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to Hyatt is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The following is a non-exhaustive list of 35 U.S.C. 112 second paragraph violations in the claims:

Claim 1:

i. the claim recites "in each frequency range" but does not define the ranges.

ii. in the second limitation, it is unclear whether the current source waveform is represented as a current source model information, or if the modeling is done as a current source device model information

iii. the term 'current source device model information' is indefinite

iv. the term 'high-speed' is indefinite, and the Examiner interprets the claimed 'high-speed Fourier transform' to be analogous to Fast Fourier Transforms (FFTs)

Claim 2:

v. it is unclear regarding what is meant by 'allocating different discrete FFT analysis frequency widths to the specified frequency range and to a frequency range other than the specified frequency range'. **This is an outstanding rejection that has not been addressed by Applicants.**

Claim 4:

vi. the phrase '...the time interval being less than a time range of to be analyzed.' What is to be analyzed? The Examiner interprets the limitations of this claim to be functionally equivalent to calculating the current frequency component at each frequency for a given time interval.

Claims 8-9:

vii. the phrase 'object network' is indefinite

Claims 10-12:

viii. the phrase 'signal logical level changing numbers' is indefinite. The Examiner believes the Applicant intended to recite the 'changing of the signal logic.' It is unclear what significance the term 'number' has on the rest of the phrase.

Claims 13 & 14:

ix. the term 'a means as a user interface' is indefinite

x. the meaning of the phrase "...an instance, which is a circuit unit, name which mainly causes noise in an associated frequency component with large noise level' is indefinite

xi. the terms 'large' and 'mainly' are indefinite

Claim 15-17 and 19:

xii. the term 'a means as a user interface' is indefinite

Claim 18:

xiii. the term 'a means as a user interface' is indefinite

xiv. the phrase '...identifying, from the instance, which is a basic circuit unit, grouping information, an instance name which mainly...' is indefinite. Are grouping information, circuit unit, and an instance name equivalent? Are they all obtained from the instance or just one of the three?

xv. the term 'large noise' is indefinite.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 1-4, 7-12, 20-34, and 36 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product.

Claim 1 is directed to analyzing the amount of electromagnetic interference of an LSI by executing a logic simulation. This claimed subject matter lacks a practical application of a judicial

exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for performing high-speed Fourier transform processing on current switching information calculated by the simulating step. This produced result remains in the abstract and, thus, fails to achieve the required status of having real world value. **Claims 2-4 and 7-12 are rejected by virtue of their dependency.**

Claim 20 is directed to analyzing the amount of electromagnetic interference of an LSI by executing a logic simulation. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for analyzing the amount of electromagnetic interference of an LSI based on the corrected event-based model of an estimated current waveform. This produced result remains in the abstract and, thus, fails to achieve the required status of having real world value. **Claims 21-25 are rejected by virtue of their dependency.**

Claim 26 is directed to analyzing the amount of electromagnetic interference of an LSI by executing a logic simulation. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a

computation, or manipulated data. More specifically, the claimed subject matter provides for simulating the EMI of the LSI by estimating the corrected event-based model of an estimated current waveform. This produced result remains in the abstract and, thus, fails to achieve the required status of having real world value. **Claims 27-24 and 36 are rejected by virtue of their dependency.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1, 3-7 and 12-19 are rejected under 35 U.S.C. 103(a)** as being unpatentable over **Hayashi et al ('EMI-Noise Analysis under ASIC Design Environment')**, herein referred to as Hayashi.

Regarding claims 1 and 3:

- **Hayashi discloses:**

  a. performing modeling of a current source waveform as a current source device modeling information **("2. Modeling")**

  b. extracting a power supply wiring **("2.1 Core Power Network Model")**

  c. simulating based on the extracted power supply wiring and the current source device model by a transient analysis simulator **("3. Simulation Flow": figure 12; 1st-3rd paragraphs).** SPICE, a transient analysis simulator, is used.

  d. performing high-speed Fourier transform processing on current switching information calculated by the simulating step **("3. Simulation Flow": 4th paragraph)**

As per **claims 1 and 3**, Hayashi discloses performing EMI-noise analysis in an ASIC design environment (**"Abstract"**). After a netlist for the *model* is generated, switching current waveforms are obtained. Logic simulation is then performed using the Verilog netlist and test vectors. Current waveforms are then obtained by superposing current waveforms in the Cell Current Waveform Library according to event data. Power network data is then extracted, and *FFTs are performed on current waveforms*.

Hayashi does not explicitly disclose performing the FFTs by first breaking the signal into frequency bins. **The Examiner maintains that it would have been obvious to a skilled artisan to perform the FFT by allocating a discrete analysis frequency in each range.** The Applicant appears to be claiming the fundamental rules of performing FFTs, as it is well known in the art that prior to performing FFT, it is necessary to divide the signal into adequately defined bins, each with a clear frequency range. See for example, **Diethorn (US Patent No. 6,035,048) column 5 line 66 – column 6 line 6**, which states:

> The N-vector of windowed data is then subjected to N-point FFT 150. As noted, this transform is effectuated, in our current implementation, using the DFT algorithm. Each frequency bin output from the DFT represents one new complex time-series sample for the sub-band frequency range corresponding to that bin. The bandwidth of each bin, or sub-band time series, is given by the ratio of sampling frequency to transform length.

The Examiner notes that it is known that a DFT produces the same result as an FFT but eliminates redundant calculations. Diethorn discloses performing FFTs using the DFT algorithm (i.e. a standard algorithm that is well-known in the art), which involves multiple frequency bins, each with a unique frequency range. See also **"Engineer to Engineer Note" section 3 'Points in FFT'** which states:

> An FFT output can be thought of as a series of bins at specific frequencies evenly spread over the range 0 to f/2 (f is the sampling frequency) with the space of f/N.

Regarding claim 4:

This functionality would inherently be included in the simulator taught by Hayashi, because the computation of the frequency component would necessarily be time based (i.e. real-time, etc).

Regarding claims 5 and 6:

Hayashi discloses storing current component values only in excess of a predetermined threshold value or in order of magnitude **(figure 10; "2.4 Switching Current Model" 3rd paragraph)**.

Regarding claim 7:

Hayashi discloses a method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes a step of calculating a current component at each frequency for only a predetermined circuit portion in a network to be analyzed **("4.1 Test Chips" (c))**. Hayashi discloses calculating current information for the clock distribution only.

Regarding claim 12:

The Examiner interprets the 'changing of signal logic' to be analogous to the switching current, the calculation of which **Hayashi discloses in section 2.4.**

Regarding claims 13-14:

Hayashi discloses calculating current component information at the instance level **("2.4 Switching Current Model")** and the circuit level **("4.1 Test Chips" (c)).**

Regarding claim 15:

Hayashi discloses grouping instanced according to flag information written in a library **("2.3 I/O Power Network Model" 4th paragraph).**

Regarding claim 16:

Hayashi discloses grouping instances according to whether the instances belong to a clock tree connected to each clock input terminal **("4.1 Test Chips" (c)).**

Regarding claim 17:

Hayashi discloses grouping instances according to a result of identifying the timing at which the instance output changes occur **("2.2 Capacitance Model").** The capacitances *(instances)* including the capacitance of the signal wire connected to the output pin are calculated.

Regarding claim 18:

Hayashi discloses identifying from the instance an instance name which mainly causes noise in an associated frequency component with large noise and then reporting information on noise level (**"4.1 Test Chips" (c)).**

Regarding claim 19:

This feature would inherently be included in method taught by Hayashi, because when performing FFTs, the frequencies are defined in advance.

6. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al ("EMI-Noise Analysis under ASIC Design Environment")**, herein referred to as Hayashi, in view of **Cheng ("Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design")**.

Regarding claims 8-11:

Hayashi does not explicitly disclose calculating a current component at each frequency for only those circuit portions in an object network having one or more circuit portions whose currents are estimated to exceed a predetermined threshold. **Chen teaches** identifying hotspots (i.e. portions that emit maximum noise or noise that is outside a certain range or above a threshold) in the circuit, and optimizing (which involves calculating their current components) them **(Chen: "6 Decap Optimization Procedure" 2nd-3rd paragraphs).** At the time of the invention, a skilled artisan would have knowingly combined the teachings of Hayashi and Chen because this minimizes switching noise **(Chen: "6 Decap Optimization Procedure" 1st paragraph). Regarding claims 10-11,** the Examiner interprets the 'changing of signal logic' to be analogous to the current waveforms (i.e. a display of the change in current), the calculation of which is taught in **section 2.4 of Hayashi and section 3 of Chen.**

7. **Claims 20-34 and 36 are rejected under 35 U.S.C. 103(a)** as being unpatentable over **Cheng ("Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design")**, in view of **Hayashi et al ("EMI-Noise Analysis under ASIC Design Environment")**, herein referred to as Hayashi.

Regarding claims 20 and 26:

Cheng discloses a method of analyzing the amount of electromagnetic interference of LSI by executing a logic simulation, the method including

a. a current waveform correction step comprising:

i. calculating an equivalent resistance and equivalent capacitance of an entire chip from a resistance and a capacitance of a power supply circuit of the chip that were determined by performing LPE based on layout data, **("2 Power Bus Model" 3rd-4th paragraphs)** and calculating a correction coefficient based on the calculated data **("6 Decap Optimization Procedure" 2nd paragraph A_n)**. First, the resistance and capacitance for each power bus segment is calculated, and this is used to calculate the resistance and capacitance for the whole on-chip power supply (i.e. the calculations are all done in an *hierarchical* manner see **"8 Conclusions**). The correction coefficient claimed is analogous to the coefficient A_n that is imposed on the layout to minimize the noise

ii. correcting, by using the correction coefficient, a model of an estimated current waveform obtained in advance **("6 Decap Optimization Procedure" 2nd paragraph).** If the constraint A_n is not met, the entire process, i.e. extraction, obtaining the current waveform **(figure 5)** is iteratively repeated until the amount of decoupling capacitors is sufficient.

b. analyzing the amount of electromagnetic interference of the LSI based on the corrected model of the current waveform (**"6 Decap Optimization Procedure" 2nd paragraph).** The process (extracting, modeling, simulating) is repeated until the circuit's EMI is acceptable.

Cheng does not explicitly disclose the use of an event-based model and an ideal power supply model. **Hayashi teaches** an event-based model **(Hayashi: "2.4 Switching Current Model" 3rd paragraph)** and an ideal power supply model **("2 Modeling").** At the time of the invention, a skilled artisan would have obviously combined the teachings of Cheng and Hayashi because the two step approach taught by Hayashi is a common approach in power distribution analysis **("2 Modeling").**

Regarding claim 21:

Cheng does not explicitly disclose the use of a table to calculate the correction coefficient. However, a skilled artisan would have knowingly implemented the calculation using a table, because it is well known in the art to use a table store values See Microsoft Computer Dictionary, 5th Edition:

> table: in programming, a data structure usually consisting a list of entries, each entry being identified by a unique key and containing a set of related values

Regarding claim 22:

Cheng discloses calculating the correction coefficient by performing processing according to a mathematical expression prepared in advance **("6 Decap Optimization Procedure" 2nd paragraph).**

Regarding claim 23:

Cheng discloses correcting the base of the current waveform **(figure 5; "6 Decap Optimization Procedure" 2nd paragraph).**

Regarding claim 24:

Cheng discloses correcting the area of the current waveform **("6 Decap Optimization Procedure" 2nd paragraph).**

Regarding claim 25:

Cheng discloses using shape information to estimate the resistance of the chip and then perform correction **("6 Decap Optimization Procedure" 1st-2nd paragraph).**

Regarding claim 27:

Cheng discloses estimating the resistance and capacitance by considering the area of the chip **("3. Switching Circuit Model" 2nd paragraph).** Cheng discloses incorporating the power *of the corresponding area.*

Regarding claim 28:

Cheng discloses estimating the resistance and capacitance by considering technology information **("5 Switching Noise Analysis" 3rd paragraph).**

Regarding claims 29-31:

The combination of Cheng and Hayashi disclose estimating the resistance and capacitance by considering a chip shape **(Chen: "6 Decap Optimization Procedure" 2nd paragraph)** and power supply pad position **(Hayashi: figure 8 two power supply pads)** and the width of the power supply wire **(Chen: "2 Power Bus Model 3rd paragraph).**

Regarding claim 32:

Chen discloses estimating the resistance and capacitance by considering a capacitance generation area under the power supply wire **(Chen: "2 Power Bus Model 3rd paragraph fringe capacitance).**

Regarding claims 33-34:

Chen discloses an electromagnetic interference analysis method according to claim 20 , wherein, to consider the power supply wire for each module in a post-layout electromagnetic interference analysis includes a step of calculating an equivalent resistance and an equivalent capacitance for each module, and calculating a correction coefficient for each module to make corrections to the estimated current waveform more precisely for each module **("3 Switching Circuit Model"; "6 Decap Optimization Procedure" 1st-2nd paragraph).**

Regarding claim 35:

Cancelled

Regarding claim 36:

Chen discloses considering an inductance component from package information corresponding to a leading and bonding portion **("2 Power Bus Model 1st–3rd paragraphs).**

Regarding claim 37:

Cancelled

Allowable Subject Matter

8. **Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable** if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and amended to overcome all 35 U.S.C. 112 and 101 rejections.

Conclusion

9. All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

Shambhavi Patel
Examiner
Art Unit 2128

KAMINI SHAH
SUPERVISORY PATENT EXAMINER